Concurrency Kit
Towards accessible scalable synchronization primitives for C
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About Me

Co-founder of Backtrace (http://backtrace.io)
Building a better debugging platform for native applications.

Started Concurrency Kit
A concurrent memory model for C99 and arsenal of tools for high performance synchronization.

Previously at AppNexus and Message Systems doing work centralized around architecture, performance and reliability. Worked on PGAS languages, multicore synchronization and parallel I/O at GWU HPCL.
Motivation
Motivation

Design and implement high performance synchronization primitives for high performance parallel software.

- A concurrent memory model for C.
- A unified interface for hardware intrinsics.

Design and implement high performance data structures.

- Safe memory reclamation mechanisms.
- Specialized concurrent data structures.

All this awesome technology has been out there for over 20 years.
Introduction

Concurrency Kit provides a concurrent memory model for C99 and arsenal of tools for high performance synchronization.

- Support for FreeBSD and Linux kernels.
- Tested with GCC, MingW, ICC, clang and SunCC. Used with several research compilers.
- Support for x86, ARM, SPARCv9+, Power.
- BSD licensed.

Likely that a text message, e-mail, image or advertisement you saw today involved Concurrency Kit.
Overview

Concurrency Primitives
- Compiler, memory ordering and primitive-operation abstraction.

Spinlocks
- Pluggable into generic cohort and elision framework.

Execution Barriers
- Primarily superseded by phasers.

Read-Write Synchronization
- Pluggable into cohort and elision framework.

Safe Memory Reclamation
- One passive and one active implementation.

Data Structures
- Array, ring buffer, bitmap, hash tables, queue, stack, etc…
Concurrency Primitives

Provides a complete partial ordering interface for interaction between stores, loads and atomic operations. Memory ordering exceptions expressed with strict fence interface.

Memory Barrier Interface

- `ck_pr_fence_atomic`
- `ck_pr_fence_atomic_load`
- `ck_pr_fence_atomic_store`
- `ck_pr_fence_store_atomic`
- `ck_pr_fence_load`
- `ck_pr_fence_load_atomic`
- `ck_pr_fence_load_store`
- `ck_pr_fence_store_load`
- `ck_pr_fence_memory`
- `ck_pr_fence_acquire`
- `ck_pr_fence_release`
- `ck_pr_fence_lock`
- `ck_pr_fence_unlock`

- `ck_pr_fence_strict_atomic`
- `ck_pr_fence_strict_atomic_load`
- `ck_pr_fence_strict_atomic_store`
- `ck_pr_fence_strict_store_atomic`
- `ck_pr_fence_strict_load_atomic`
- `ck_pr_fence_strict_load_store`
- `ck_pr_fence_strict_store_load`
- `ck_pr_fence_strict_memory`
- `ck_pr_fence_strict_acquire`
- `ck_pr_fence_strict_release`
- `ck_pr_fence_strict_lock`
- `ck_pr_fence_strict_unlock`

These are the lowest common denominator and can serve as building blocks for FreeBSD/C11-style acquire-release semantics.
Concurrence Primitives

The memory model and instruction set are decoupled. Porters transcribe a handful of operations from architecture manuals and rarely have to concern themselves with memory model minutiae and additional boilerplate.

Native load, store, atomic operations and strict fences.
Concurrence Primitives

The memory model and instruction set are decoupled. Porters transcribe a handful of operations from architecture manuals and rarely have to concern themselves with memory model minutiae and additional boilerplate.
Concurrency Primitives

All concurrent accesses on actively mutable state are annotated with ck_pr operations that expand to the necessary hardware instructions and also serve as a compiler barrier.

- **volatile** does not provide any atomicity guarantees and ordering is only defined with respect to other volatile accesses.
- **volatile** unnecessarily disables a lot of optimizations.
Concurrency Primitives

Some notable primitives that are applicable to FreeBSD.

- Type-safe interaction with pointers in master (no need to play casting games with long) using only C99, true assignment semantics.*
  - struct a *a; struct b *b; ck_pr_store_ptr(&a, b) is invalid.
- **ck_pr_rfo**
  - Read-for-ownership primitive was once AMD only, now available in Intel Broadwell+ (compatible).
  - Drastic reduction in cache-coherency traffic for prefetchable workloads.
- **ck_pr_rtm**
  - Restricted transactional memory now available on Intel (Haswell+ for broken version, recent Broadwell for fixed version) and Power 8+.
  - Scalability for qualifying workloads (fast path cost slightly more expensive than atomic and high abort cost).

* Thanks to pkhuong and jwittrock for the store and load coverage.
Concurrency Primitives

Future work is to provide MD-agnostic acquire-release interface similar to C11/FreeBSD interface.

Questions?
Spinlocks

A myriad of spinlock implementations with varying fairness and scalability guarantees.

<table>
<thead>
<tr>
<th></th>
<th>Fair</th>
<th>Scalable</th>
<th>Fast Path</th>
<th>Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>ck_anderson</td>
<td>1A1F</td>
<td>o(N)</td>
<td>1A1F</td>
<td>o(N)</td>
</tr>
<tr>
<td>ck_cas</td>
<td>1A0F</td>
<td>o(1)</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_clh</td>
<td>1A1F</td>
<td>o(N)</td>
<td>1A1F</td>
<td>o(N)</td>
</tr>
<tr>
<td>ck_dec</td>
<td>1A0F</td>
<td>o(1)</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_fas</td>
<td>1A0F</td>
<td>o(1)</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_hclh*</td>
<td>1A2F</td>
<td>o(N)</td>
<td>1A2F</td>
<td>o(N)</td>
</tr>
<tr>
<td>ck_mcs</td>
<td>2A1F</td>
<td>o(N)</td>
<td>2A1F</td>
<td>o(N)</td>
</tr>
<tr>
<td>ck_ticket</td>
<td>2A0F</td>
<td>o(1)</td>
<td>2A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>struct mtx</td>
<td>1A0F</td>
<td>o(1)</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
</tbody>
</table>

Fast path is tuple nAkF where n is number of atomics and k is number of fences (ignoring necessary lock fence).

* Thanks to cognet@ for ck_hclh work.
Spinlocks

Starvation-freedom and fairness are especially important on NUMA, and pretty much everything that isn’t small-form is NUMA.

But if there is non-negligible jitter, fairness does cost system-wide throughput.
Spinlocks

A scalable lock may sound like a misnomer, but an unscalable lock will **degrade** performance under contention.

Spinlocks

These algorithms apply to adaptive locks, they optimize busy-wait stage while providing stronger fairness guarantees.

Questions?
Elision

Later Intel x86 and Power 8 processors support restricted transactional memory (RTM). The typical use-case is lock elision.

Thread 0
ck_spinlock_lock(&lock);
array[0] = 1;
ck_spinlock_unlock(&lock);

Thread 1
ck_spinlock_lock(&lock);
array[1291] = 1;
ck_spinlock_unlock(&lock);
Elision

Later Intel x86 and Power 8 processors support restricted transactional memory (RTM). The typical use-case is lock elision.

Thread 0
CK_ELIDE_LOCK(yo, &lock);
array[0] = 1;
CK_ELIDE_UNLOCK(yo, &lock);

Thread 1
CK_ELIDE_LOCK(yo, &lock);
array[1291] = 1;
CK_ELIDE_UNLOCK(yo, &lock);
Elision

Questions?
Cohorts

Turn any lock into a NUMA-aware lock without sacrificing throughput. At least 2 additional atomic operations on fast path, not competitive on commodity multicore systems.

Questions? Talk to Brendon, he’s here.
Execution Barriers

Prevents execution at a barrier until all threads have paired*. A plethora of implementations from the literature. Scalability is usually not a concern.

Questions? Let’s talk later.

* Thanks to djoseph for work on these.
Blocking Asymmetric Synchronization

The most common form of asymmetric synchronization is the read-write lock.

<table>
<thead>
<tr>
<th>Type</th>
<th>Bias</th>
<th>Fair</th>
<th>Scalable</th>
<th>Reader Fast Path</th>
<th>Space</th>
</tr>
</thead>
<tbody>
<tr>
<td>rwlock</td>
<td>WB</td>
<td>No</td>
<td>No</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>rmlock</td>
<td>WB*</td>
<td>No</td>
<td>Yes</td>
<td>0</td>
<td>o(N)</td>
</tr>
<tr>
<td>ck_brlock_t</td>
<td>WB*</td>
<td>No</td>
<td>Yes</td>
<td>1A1F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_rwlock_t</td>
<td>WB</td>
<td>No</td>
<td>No</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_bytelock_t</td>
<td>WB</td>
<td>No</td>
<td>No</td>
<td>0A1F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_pflock_t</td>
<td>None</td>
<td>Phase</td>
<td>No</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_tflock_t*</td>
<td>None</td>
<td>Yes</td>
<td>No</td>
<td>1A1F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_sequence_t</td>
<td>WB*</td>
<td>No</td>
<td>No</td>
<td>0A1F</td>
<td>o(1)</td>
</tr>
<tr>
<td>ck_swlock_t</td>
<td>WB</td>
<td>No</td>
<td>No</td>
<td>1A0F</td>
<td>o(1)</td>
</tr>
</tbody>
</table>

* Thanks to jwittrock for ck_tflock work and jsridhar for ck_swlock_t work.
Blocking Asymmetric Synchronization

Task-fair and phase-fair locks provide nicer scheduling guarantees between readers and writers. They can augment adaptive paths.

Source: Spin-Based Reader-Writer Synchronization for Multiprocessor Real-Time Systems by Brandenburg and Anderson
ck_sequence_t is a simple blocking primitive that allows for concurrently reading data without interfering with writers. Readers may spin indefinitely.

```c
void reader(void)
{
    struct example copy;
    unsigned int version;

    CK_SEQUENCE_READ(&seqlock, &version) {
        copy = global;
    }

    return;
}
```
Blocking Asymmetric Synchronization

The fairness and performance trade-offs are elaborated in manual pages.

Questions?
Legal Break

Nothing in this presentation constitutes legal advice. Consult with a lawyer, accountant, and insurance professional before making your decisions. The views and opinions in this presentation represent my own and not those of people, institutions or organizations I am affiliated with unless stated explicitly. This presentation does not represent the views, position or attitudes of my employer, their clients, or any of their affiliated companies.
Blocking Asymmetric Synchronization

Any non-negligible amount of write workload leads to performance degradation of readers.

If liveness and reachability of object is decoupled with blocking synchronization, techniques like reference counting must be used. Reference counting with atomics is expensive.
Safe Memory Reclamation

Safe memory reclamation protects against read-reclaim races with minimal to no interference to readers.
Safe Memory Reclamation

Safe memory reclamation protects against read-reclaim races with minimal to no interference to readers.
Safe Memory Reclamation

The most popular form of safe memory reclamation these days is RCU. Unfortunately, the patent exemption only applies to LGPL and GPL software.

<table>
<thead>
<tr>
<th></th>
<th>Fast Path</th>
<th>Traversal</th>
<th>Amortization</th>
</tr>
</thead>
<tbody>
<tr>
<td>ck_hp</td>
<td>nA l nF</td>
<td>Expensive</td>
<td>Expensive</td>
</tr>
<tr>
<td>ck_epoch</td>
<td>1A l 1F</td>
<td>Fast</td>
<td>Amortized</td>
</tr>
<tr>
<td>QSBR</td>
<td>0</td>
<td>Fast</td>
<td>Fast</td>
</tr>
</tbody>
</table>
## Safe Memory Reclamation

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>1st Qu.</th>
<th>Median</th>
<th>Mean</th>
<th>3rd Qu.</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epoch</td>
<td>72</td>
<td>76</td>
<td>76</td>
<td>204</td>
<td>236</td>
<td>53350</td>
</tr>
<tr>
<td>RCU</td>
<td>136</td>
<td>144</td>
<td>144</td>
<td>375</td>
<td>572</td>
<td>264600</td>
</tr>
<tr>
<td>QSBR</td>
<td>128</td>
<td>136</td>
<td>136</td>
<td>248</td>
<td>224</td>
<td>54330</td>
</tr>
<tr>
<td>Signal</td>
<td>44</td>
<td>44</td>
<td>44</td>
<td>62.35</td>
<td>48</td>
<td>63930</td>
</tr>
</tbody>
</table>
# Safe Memory Reclamation

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>1st Qu.</th>
<th>Median</th>
<th>Mean</th>
<th>3rd Qu.</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epoch</td>
<td>72</td>
<td>100</td>
<td>484</td>
<td>619</td>
<td>940</td>
<td>551300</td>
</tr>
<tr>
<td>RCU</td>
<td>136</td>
<td>144</td>
<td>296</td>
<td>414</td>
<td>636</td>
<td>412800</td>
</tr>
<tr>
<td>QSBR</td>
<td>128</td>
<td>136</td>
<td>220</td>
<td>287</td>
<td>380</td>
<td>43050</td>
</tr>
</tbody>
</table>
## Safe Memory Reclamation

<table>
<thead>
<tr>
<th></th>
<th>Min</th>
<th>1st Qu.</th>
<th>Median</th>
<th>Mean</th>
<th>3rd Qu.</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epoch</td>
<td>188</td>
<td>772</td>
<td>1408</td>
<td>1781</td>
<td>2348</td>
<td>1888000</td>
</tr>
<tr>
<td>RCU</td>
<td>720</td>
<td>9260</td>
<td>26610</td>
<td>44080</td>
<td>60670</td>
<td>2181000</td>
</tr>
<tr>
<td>QSBR</td>
<td>400</td>
<td>10130</td>
<td>25420</td>
<td>38250</td>
<td>53590</td>
<td>4526000</td>
</tr>
</tbody>
</table>
Safe Memory Reclamation

Questions?
**Ring Buffer**

**ck_ring_t** is a lock-free ring buffer in Concurrency Kit. It is wait-free for single-producer / single-consumer and lock-free for single-producer / multi-consumer.

<table>
<thead>
<tr>
<th></th>
<th>buf_ring_t</th>
<th>ck_ring_t</th>
</tr>
</thead>
<tbody>
<tr>
<td>Correct</td>
<td>No (but most fixes in review)</td>
<td>Yes</td>
</tr>
<tr>
<td>SPMC</td>
<td>Serialized</td>
<td>Wait-Free / Lock-Free</td>
</tr>
<tr>
<td>MPSC</td>
<td>Serialized</td>
<td>N/A</td>
</tr>
<tr>
<td>SPSC</td>
<td>Wait-Free</td>
<td>Wait-Free</td>
</tr>
<tr>
<td>MPMC</td>
<td>Serialized</td>
<td>N/A (Serialized / Lock-Free)</td>
</tr>
<tr>
<td>Multibyte Storage</td>
<td>No</td>
<td>Yes</td>
</tr>
</tbody>
</table>

Serialized transformation with **buf_ring_t** fast path cost is easy to add, **ck_ring_t** counter representation would not require serializing consumer.
Hash Table

General technique for achieving lock-free / wait-free single-writer / many-reader open-addressed hash table with practically **0 cost** for TSO and sometimes low-cost for RMO. Applicable even in absence of safe memory reclamation techniques.

<table>
<thead>
<tr>
<th>Data Structure</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>ck_hs</td>
<td>Hash set (cache line to double hash)</td>
</tr>
<tr>
<td>ck_rhs*</td>
<td>Hash set (robin hood hash)</td>
</tr>
<tr>
<td>ck_ht</td>
<td>Hash table (cache line to double hash)</td>
</tr>
</tbody>
</table>

* Thanks to cognet@ for ck_rhs
Hash Table

A ck_ht replacement is in the works.

Questions?
The End

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http://backtrace.io

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